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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,063	08/12/2008	Stefan Peter Grabowski	DE04 0001 US1	6197

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
LULIS, MICHAEL P	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
06/23/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/585,063	GRABOWSKI ET AL.	
	Examiner	Art Unit	
	MICHAEL LULIS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/29/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 06/29/2006 has been considered.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Jacobson et al. (US 6294401 B1, hereinafter Jacobson).**

6. **Regarding claim 1**, Jacobson discloses a semiconductor component which is arranged in a semiconductor body, with at least one source zone (fig. 7: 720s) and with at least one drain zone (fig. 7: 720d) of in each case a first conductivity type, with at least one body zone (fig. 7: 710) of a second conductivity type arranged in each case between source zone and drain zone, and with at least one gate electrode (fig. 7: 730) insulated from the semiconductor body by means of an insulating layer (fig. 7: 720), the insulating layer being a consolidated layer containing quantum dots (col. 8 ll. 15-19).

7. **Regarding claim 2**, Jacobson discloses a semiconductor component as claimed in claim 1 (see above), characterized in that the consolidated insulating layer contains quantum dots embedded in a matrix of a dielectric material (col. 8 ll. 15-19).

8. **Regarding claim 4**, Jacobson discloses a semiconductor component as claimed in claim 1 (see above), characterized in that the consolidated insulating layer 9 is a sintered layer (col. 8 ll. 15-19).

9. **Regarding claim 5**, Jacobson discloses a method of manufacturing a semiconductor component which is arranged in a semiconductor body, with at least one source zone (fig. 7: 720s) and with at least one drain zone (fig. 7: 720d) of in each case a first conductivity type, with at least one body zone (fig. 7: 710) of a second conductivity type arranged in each case between source zone and drain zone, and with at least one gate electrode (fig. 7: 730) insulated from the semiconductor body by means of a consolidated insulating layer containing quantum dots (col. 8 ll. 15-19), in which method the consolidated insulating layer is produced by applying a suspension containing quantum dots to the semiconductor body and consolidating it.

10. **Regarding claim 6**, Jacobson discloses a method as claimed in claim 5 (see above), characterized in that consolidation of the insulating layer is effected by means of sintering (col. 8 ll. 15-19).

11. **Regarding claim 7**, Jacobson discloses a method as claimed in claim 5 (see above), characterized in that the suspension additionally contains particles of a dielectric material, wherein the diameter of the particles of the dielectric material is smaller than the diameter of the quantum dots (col. 3 ll. 35-43).

12. **Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Flagan et al. (US 20020074565 A1, hereinafter Flagan).**

13. **Regarding claim 1**, Flagan discloses a semiconductor component which is arranged in a semiconductor body, with at least one source zone (fig. 10: 122) and with at least one drain zone (fig. 10: 122) of in each case a first conductivity type, with at least one body zone (fig. 10: 74) of a second conductivity type arranged in each case between source zone and drain zone, and with at least one gate electrode (fig. 10: 132) insulated from the semiconductor body by means of an insulating layer (fig. 10: 101), the insulating layer being a consolidated layer containing quantum dots (fig. 10: 102).

14. **Regarding claim 2**, Flagan discloses a semiconductor component as claimed in claim 1 (see above), characterized in that the consolidated insulating layer contains quantum dots (fig. 10: 102) embedded in a matrix of a dielectric material (para [0056]).

15. **Regarding claim 3**, Flagan discloses a semiconductor component as claimed in claim 1 (see above), characterized in that the quantum dots contain a semiconductor material (para [0056]).

16. **Regarding claim 4**, Flagan discloses a semiconductor component as claimed in claim 1 (see above), characterized in that the consolidated insulating layer 9 is a sintered layer (para [0031]).

17. **Regarding claim 5**, Flagan discloses a method of manufacturing a semiconductor component which is arranged in a semiconductor body, with at least one source zone (fig. 10: 122) and with at least one drain zone (fig. 10: 122) of in each case a first conductivity type, with at least one body zone (fig. 10: 74) of a second conductivity type arranged in each case between source zone and drain zone, and with at least one gate electrode (fig. 10: 132) insulated from the semiconductor body by means of a consolidated insulating layer (fig. 10: 101) containing quantum dots (fig. 10: 101), in which method the consolidated insulating layer is produced by applying a suspension containing quantum dots to the semiconductor body and consolidating it (para [0056]).

Conclusion

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Lulis whose telephone number is (571) 272-

9015. The examiner can normally be reached on 8:30 AM to 5:00 PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael Lulis/
Examiner, Art Unit 2824

/ANH PHUNG/

Primary Examiner, Art Unit 2824